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100G CFP2 to QSFP28 Adapter Module, Dual-Rate

Part Number: FADP-AS8-C2QP-Nx

Overview

The 100G CFP2 to QSFP28 Adapter module, FADP-AS8-C2QP, is a four-channel, high performance, hot pluggable and ideal interconnect solution supporting 100G Ethernet and OTN OTU4. It converts CFP MSAinterface to 1-port 100GE QSFP28 and integrates four data lanes in each direction with operating data rate up to 28Gbps per lane. FADP-AS8-C2QP has no FEC function itself but it could support 100G QSFP28 LR4 / ER4 modules without FEC. When the 100GE host equipment has FEC function on CFP2 port, it could support 100G QSFP28 SR4 / PSM4 / CWDM4 / CLR4 modules. FADP-AS8-C2QP work with Low power consumption <2W and is RoHS compliant.

Applications

- IEEE 802.3ba 100GBASE-LR4 / ER4 Ethernet
- 100GE interconnects for QSFP28 SR4 / PSM4 / CWDM4, CLR4 when CFP2 port with FEC.
- Data aggregation and backplane application
- High speed core router connection and
- Datacom / Telcom switch

Features

- Compliant with CFP2 Hardware Specification Version 1.0
- Compliant with CFP Management Interface Specification Version 2.4
- 4 Full-Duplex channels
- Internal CDR on Transmitters and Receivers
- Transmission data rate up to 28Gpbs per channel
- OTU4 compatible
- Without FEC (Forward Error Correction)
- 1 port QSFP28 Tx&Rx
- MDIO digital diagnostic interface
- Hot Pluggable
- Single +3.3V power supply
- Power Class 3 (Adapter only <2W)
- Operating case temperature 0 ~ +70°C
- RoHS compliant

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Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit
Storage Temperature	T_{ST}	-20	+85	°C
Storage Relative Humidity	RH	5	85	%
Supply Voltage	V_{CC}	-0.5	+3.6	V

Recommended Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Unit
Operating Case Temperature	T_{OP}	0	-	+70	°C
Supply Voltage	V_{CC}	+3.13	+3.3	+3.47	V
Maximum Power Dissipation	P			2	W
Data Rate per Lane			25.78125	27.952	Gbps
Aggregate Data Rate			103.125	111.8	Gbps

Note1: The maximum power dissipation is the total of the adapter without QSFP28 transceiver.

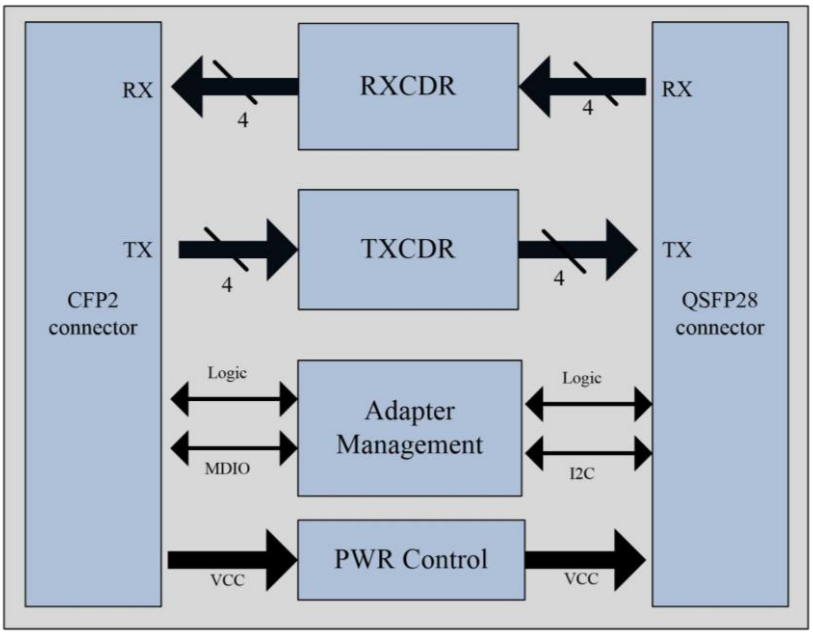
Electrical Characteristics

V_{CC}= 3.13V to 3.47V, T_{OP} = 0 °C to 70 °C

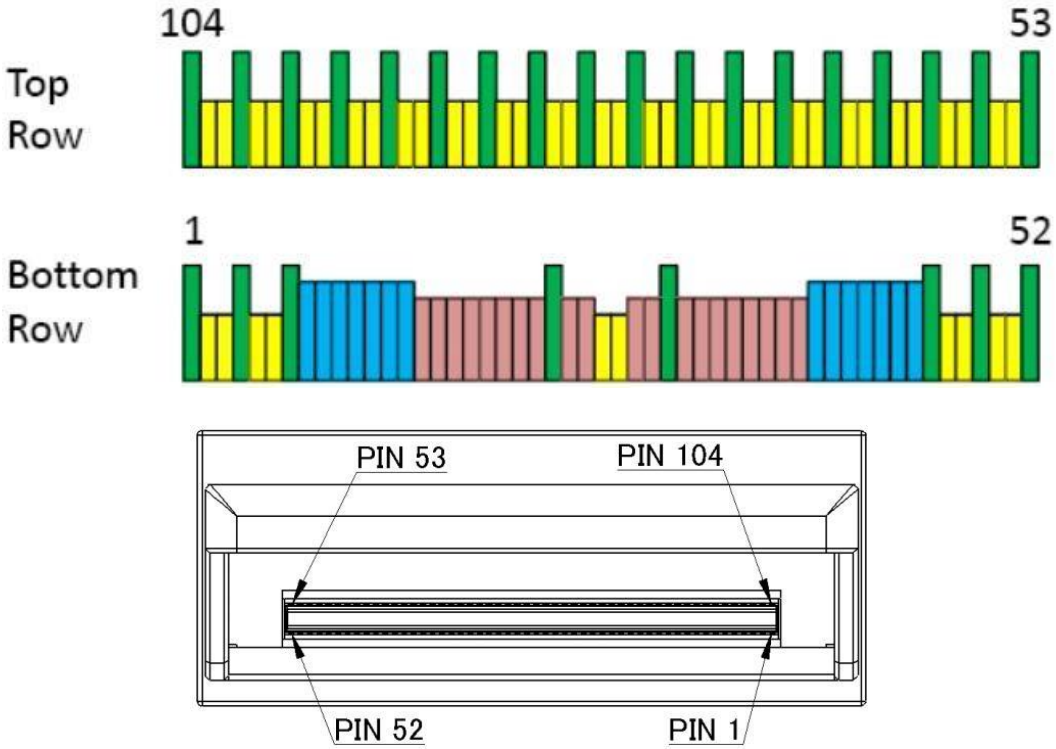
Parameters	Symbol	Min.	Typ.	Max.	Unit	Note
Differential Input Impedance	Z_{IN}	90	100	110	Ω	
Differential Output Impedance	Z_{OUT}	90	100	110	Ω	
Differential Data Input Amplitude @25GbE	V_{IN-P-P}	300		900	mVpp	1
Differential Data Output mplitude@25GbE	$V_{OUT-P-P}$	400		800	mVpp	2
Bit Error Rate	BER		10^{-12}			3
Input Logic Level High	V_{IH}	2.0		Vcc+0.3	V	4
		0.84		1.5	V	5
Input Logic Level Low	V_{IL}	-0.3		0.8	V	4
		-0.3		0.36	V	5
Output Logic Level High	V_{OH}	Vcc-0.2		Vcc	V	4
		1.0		1.5	V	5
Output Logic Level Low	V_{OL}	0		0.2	V	4
		-0.3		0.2	V	5

Note1: Differential input voltage amplitude is measured between TxnP and TxnN.
Note2: Differential output voltage amplitude is measured between RxnP and RxnN.
Note3: BER=10^{-12} ; PRBS 2^{31}-1 pattern @25.78125Gb/s.
Note4: 3.3V LVCOMS.
Note5: 1.2V LVCMOS.

Adapter Block Diagram



CFP2 Pin Assignment



CFP2 Pin Description

Bottom Row Pin Function Definition

Pin	Logic	Name	Function / Description
1		GND	Module Ground
2	CML-O	(Tx_MCLKn)	CML For optical waveform testing. Not used.
3	CML-O	(Tx_MCLKp)	CML For optical waveform testing. Not used.
4		GND	Module Ground
5		NC	No Connect
6		NC	No Connect
7		GND	3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
8		3.3V_GND	
9		3.3V	3.3V Module power Supply
10		3.3V	
11		3.3V	
12		3.3V	
13		3.3V_GND	
14		3.3V_GND	
15	I/O	VND_IO_A	Module vendor I/O A.
16	I/O	VND_IO_B	Module vendor I/O B.
17	LVCMOS-I w/PU	PRG_CNTL1	Programmable Control 1 set via MDIO, MSA default: TRxIC_RSTn – Tx & Rx IC reset. “0” = reset, “1” or NC = enabled or not used
18	LVCMOS-I w/PU	PRG_CNTL2	Programmable Control 2 set via MDIO, MSA default: Hardware Interlock LSB, “00” ≤3W, “01” ≤6W, “10” ≤9W, “11” or NC ≤12W= not used
19	LVCMOS-I w/PU	PRG_CNTL3	Programmable Control 3 set via MDIO, MSA default: Hardware Interlock MSB, “00” ≤3W, “01” ≤6W, “10” ≤9W, “11” or NC ≤12W= not used
20	LVCMOS-O	PRG_ALRM1	Programmable Alarm 1 set via MDIO, MSA default:HIPWR_ON, “1” = Module high power up completed, “0” = Module not high powered up
21	LVCMOS-O	PRG_ALRM2	Programmable Alarm 2 set via MDIO,MSA default: MOD_READY,“1” = ready, “0” = not ready
22	LVCMOS-O	PRG_ALRM3	Programmable Alarm 3 set via MDIO, MSA default: MOD_FAULT, module fault detected, “1” = fault, “0” = no fault
23		GND	Module Ground

24	Tx_DIS-I	Tx_DIS	Transmitter Disable for all channels, “1” or NC = transmitter disabled, “0” = transmitter enabled
25	Rx_LOS-O	Rx_LOS	Receiver loss of optical signal on any channel, “1” = loss of signal, “0” = normal condition
26	LVCMOS w/PU	MOD_LOPWR	Module low power mode. “1” or NC = module in low power (safe) mode, “0” = power-on enabled
27	GND	MOD_ABS	Module Absent. “1” or NC = Module absent, “0” = module present. Pull-up resistor on Host
28	LVCMOS w/PD	MOD_RSTn	Module Reset. “0” = reset the module, “1” or NC = module enabled, Pull-down resistor in module
29	LVCMOS	GLB_ALRMn	Global Alarm. “0” = alarm condition in any MDIO alarm register, “1” = no alarm. Pull-up resistor on Host
30		GND	
31	1.2V CMOS-I	MDC	Management data clock (electrical specs as per IEEE 802.3-2012)
32	1.2V CMOS-I/O	MDIO	Management Data I/O bi-directional data (electrical specs as IEEE 802.3-2012)
33	1.2V CMOS-I	PRTADR0	MDIO port address bit 0
34	1.2V CMOS-I	PRTADR1	MDIO port address bit 1
35	1.2V CMOS-I	PRTADR2	MDIO port address bit 2
36	I/O	VND_IO_C	Module vendor I/O C.
37	I/O	VND_IO_D	Module vendor I/O D.
38	I/O	VND_IO_E	Module vendor I/O E.
39		3.3V_GND	
40		3.3V_GND	
41		3.3V	3.3V Module power Supply
42		3.3V	
43		3.3V	
44		3.3V	
45		3.3V_GND	
46		GND	Module Ground
47	CML-O	NC	Received data output
48	CML-O	NC	Received data output
49		GND	Module Ground
50	CML-O	(Rx_MCLKn)	CML For optical waveform testing. Not used.

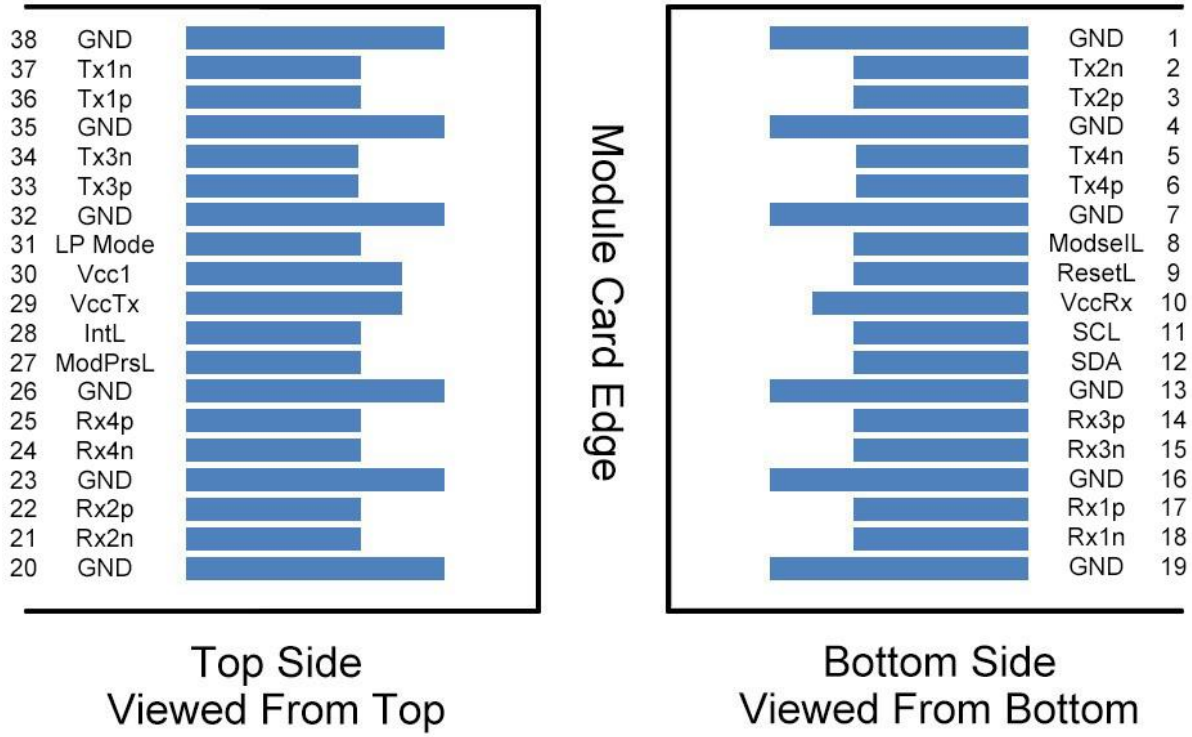
51	CML-O	(Rx_MCLKP)	CML For optical waveform testing. Not used.
52		GND	Module Ground

Top Row Pin Function Definition

Pin	Logic	Name	Function / Description
53		GND	Module Ground
54		NC	No Connect
55		NC	No Connect
56		GND	Module Ground
57	CML-O	Rx1p	Receiver Non-Inverted Data Output
58	CML-O	Rx1n	Receiver Inverted Data Output
59		GND	Module Ground
60	CML-O	Rx2p	Receiver Non-Inverted Data Output
61	CML-O	Rx2n	Receiver Inverted Data Output
62		GND	Module Ground
63		NC	No Connect
64		NC	No Connect
65		GND	Module Ground
66		NC	No Connect
67		NC	No Connect
68		GND	Module Ground
69	CML-O	Rx3p	Receiver Non-Inverted Data Output
70	CML-O	Rx3n	Receiver Inverted Data Output
71		GND	Module Ground
72	CML-O	Rx4p	Receiver Non-Inverted Data Output
73	CML-O	Rx4n	Receiver Inverted Data Output
74		GND	Module Ground
75		NC	No Connect
76		NC	No Connect
77		GND	Module Ground
78		(REFCLKp)	Not used
79		(REFCLKn)	Not used
80		GND	Module Ground
81		NC	No Connect

82		NC	No Connect
83		GND	Module Ground
84	CML-I	Tx1p	Transmitter Non-Inverted Data Input
85	CML-I	Tx1n	Transmitter Inverted Data Input
86		GND	Module Ground
87	CML-I	Tx2p	Transmitter Non-Inverted Data Input
88	CML-I	Tx2n	Transmitter Inverted Data Input
89		GND	Module Ground
90		NC	No Connect
91		NC	No Connect
92		GND	Module Ground
93		NC	No Connect
94		NC	No Connect
95		GND	Module Ground
96	CML-I	Tx3p	Transmitter Non-Inverted Data Input
97	CML-I	Tx3n	Transmitter Inverted Data Input
98		GND	Module Ground
99	CML-I	Tx4p	Transmitter Non-Inverted Data Input
100	CML-I	Tx4n	Transmitter Inverted Data Input
101		GND	Module Ground
102		NC	No Connect
103		NC	No Connect
104		GND	Module Ground

QSFP28 Pin Assignment



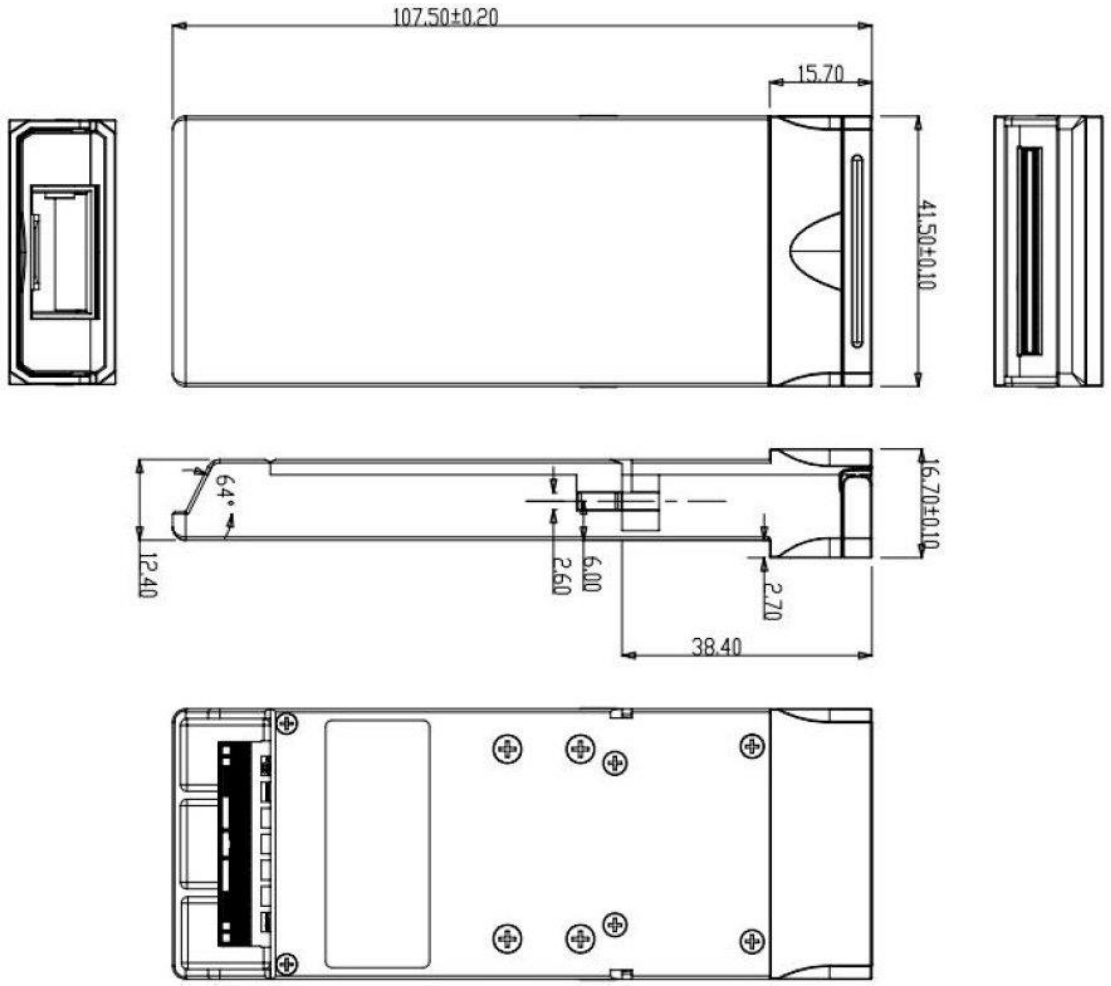
QSFP28 Pin Description

Pin	Logic	Name	Function / Description
1		GND	Module Ground
2	CML-O	Tx2n	Transmitter Inverted Data output
3	CML-O	Tx2p	Transmitter Non-Inverted Data output
4		GND	Module Ground
5	CML-O	Tx4n	Transmitter Inverted Data output
6	CML-O	Tx4p	Transmitter Non-Inverted Data output
7		GND	Module Ground
8	LVTLL-O	ModSelL	Module Select
9	LVTLL-O	ResetL	Module Reset
10		VccRx	+3.3V Power Supply Receiver
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data

13		GND	Module Ground
14	CML-I	Rx3p	Receiver Non-Inverted Data Input
15	CML-I	Rx3n	Receiver Inverted Data Input
16		GND	Module Ground
17	CML-I	Rx1p	Receiver Non-Inverted Data Input
18	CML-I	Rx1n	Receiver Inverted Data Input
19		GND	Module Ground
20		GND	Module Ground
21	CML-I	Rx2n	Receiver Inverted Data Input
22	CML-I	Rx2p	Receiver Non-Inverted Data Input
23		GND	Module Ground
24	CML-I	Rx4n	Receiver Inverted Data Input
25	CML-I	Rx4p	Receiver Non-Inverted Data Input
26		GND	Module Ground
27	LVTLL-I	ModPrsL	Module Present, QSFP28 Module pulled down to GND
28	LVTLL-I	IntL	Interrupt
29		VccTx	+3.3V Power Supply Transmitter
30		Vcc1	+3.3V Power Supply
31	LVTLL-O	LPMode	Low Power Mode
32		GND	Module Ground
33	CML-O	Tx3p	Transmitter Non-Inverted Data Output
34	CML-O	Tx3n	Transmitter Inverted Data Output
35		GND	Module Ground
36	CML-O	Tx1p	Transmitter Non-Inverted Data Output
37	CML-O	Tx1n	Transmitter Inverted Data Output
38		GND	Module Ground

Note1: Module circuit ground is isolated from module chassis ground within the module.
Note2: Open collector; pulled up within 4.7k ohms on the adaptor board to a voltage 3.3V.

Mechanical Dimensions



(All Dimensions are ±0.20mm Unless Otherwise Specified, Unit: mm)

Ordering Information

Part No.	Product Description	Temp.
FADP-AS8-C2QP-Nx	100G CFP2 to QSFP28 Adapter w/o FEC, supports 100G QSFP28 LR4 / ER4. Supports 100G QSFP28 SR4/PSM4 / CWDM4 / CLR4 when the 100GE host equipment has FEC function on CFP2 port. x= to denote the Compatibility function.	0 ~+70°C